WHAT IS CLAIMED IS:

1. A memory interlace-checking method to detect weakened memory, which comprises:

a main step, which has at least one main address accessing datum and commands to perform actions on each memory address;

a data checking step, which includes an address accessing datum containing data checking commands that check data in part of the addresses complementary to the main address accessing datum.

2. The method of claim 1, wherein the main step performs command actions on interlacing memory rows.

3. The method of claim 1, wherein the main step performs command actions on interlacing memory columns.

4. A memory interlace-checking method to detect weakened memory, which is implemented in a test program with a command action, the test program comprising:

at least a portion of main address accessing data; and

at least a portion of secondary address accessing data, which is at least partially complementary to the portion of main address accessing data.

5. The method of claim 4, wherein the main address accessing data contains the command action.

6. The method of claim 4, wherein the secondary address accessing data contains a checking action.

7. A memory interlace-checking method to detect weakened memory, which comprises:

an access step, which contains at least a main address accessing datum to perform command actions on the odd (even) address units of memory;

a checking step, which contains at least an address accessing datum and check data stored in the even (odd) address units of memory that have yet to be accessed in the access step.

8. The method of claim 7, wherein the address unit is a row.

9. The method of claim 7, wherein the address unit is a column.

10. The method of claim 7, wherein the checking step contains a checking command.